

What is claimed is:

[Claim 1] 1. A method for changing a selectable divisor in a programmable frequency divider, the frequency divider comprising a plurality of cascaded cells, the method comprising:

- (a) providing a plurality of divisor signals;
- (b) selectively switching each of the plurality of cells to a divide-by-two or a divide-by-three mode according to the plurality of divisor signals; and
- (c) synchronously resetting at least a part of the plurality of cells.

[Claim 2] 2. The method of claim 1, wherein step (c) further comprises synchronously resetting all of the plurality of cells.

[Claim 3] 3. The method of claim 1, wherein step (c) further comprises reloading the plurality of divisor signals to the plurality of cells.

[Claim 4] 4. The method of claim 3, further comprising synchronously reloading the plurality of divisor signals to the plurality of cells.

[Claim 5] 5. The method of claim 3, wherein the plurality of cells comprises at least one cell having a bypass mode, the method further comprising:

- determining whether to bypass at least a part of the at least one cell having a bypass mode according to the plurality of divisor signals in order to inhibit bypassed cells from performing a frequency-dividing operation.

[Claim 6] 6. The method of claim 5, wherein step (c) further comprises synchronously resetting each bypassed cell.

[Claim 7] 7. The method of claim 5, wherein step (c) further comprises synchronously resetting the plurality of cells.

[Claim 8] 8. The method of claim 5, wherein the reloading step further comprises synchronously reloading the corresponding divisor signals to the bypassed cells.

[Claim 9] 9. The method of claim 5, wherein the reloading step further comprises synchronously reloading the plurality of divisor signals to the plurality of cells.

[Claim 10] 10. The method of claim 5, further comprising:
utilizing a control circuit coupled to the bypassed cells for providing a reset signal.

[Claim 11] 11. The method of claim 5, further comprising:
utilizing a control circuit coupled to each of the plurality of cells for providing a reset signal.

[Claim 12] 12. The method of claim 11, wherein step (c) further comprises utilizing the control circuit to output the reset signal to the bypassed cells and a cell having a bypass mode which is prior to the bypassed cells, the reset signal being output after the bypassed cells are loaded with the corresponding divisor signals.

[Claim 13] 13. The method of claim 5, wherein step (c) further comprises bypassing a cell having a bypass mode when divisor signals input to the cell and each of its subsequent cells having a bypass mode are logic 0.

[Claim 14] 14. A programmable frequency divider for dividing the frequency of a source signal according to a selectable divisor which is obtained based on a plurality of divisor signals and outputting a result signal having a divided frequency, the programmable frequency divider comprising:

at least one cell of a first type being switchable between divide-by-two and divide-by-three modes having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (Rs), a first output node (Fo), and a second output node (Mo), the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (Rs) being used for receiving a reset signal to synchronously reset the cell of the first type;

wherein if the programmable frequency divider comprising a plurality of cells of the first type, the cells of the first type being cascaded with each other, the first output node (Fo) being coupled to a first input node (Fi) of a subsequent cell of the first type, the second input node (Mi) being coupled to a second output node (Mo) of the subsequent cell of the first type, a first input node (Fi) of a first cell of the first type being coupled to the source signal, and a second input node (Mi) of a last cell of the first type being set to logic 1; the programmable frequency divider synchronously resets all of the cells of the first type according to the reset signal in order to selectively switch each cell of the first type to perform a divide-by-two or divide-by-three operation according to the respective divisor signal after the cell is reset, and the second output node (Mo) or the first output node (Fo) of the last cell of the first type outputs the result signal having the divided frequency.

[Claim 15] 15. The programmable frequency divider of claim 14 wherein each cell of the first type operates such that:

- (a) regardless of the logic level of the second input node (Mi), if the first output node (Fo) and the third input node (Di) are both at logic 0, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the second input node (Mi) and the third input node (Di) are both at logic 1 and the first output node (Fo) is at logic 0, the positive edge of the clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal; and
- (e) if the reset signal received on the fourth input node (Rs) is enabled, the first output node (Fo) outputs a logic 0 signal and, additionally, if the second input node (Mi) is at logic 1, the second output node (Mo) outputs a logic 1 signal.

[Claim 16] 16. The programmable frequency divider of claim 14 wherein each cell of the first type operates such that:

- (a) regardless of the logic level of the second output node (Mo), if the third input node (Di) is at logic 0, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the second output node (Mo) and the third input node (Di) are both at logic 1, the positive edge of the clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;

- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal; and
- (e) if the reset signal received in the fourth input node (Rs) is enabled, the first output node (Fo) outputs a logic 0 signal; and, additionally, if the second input node (Mi) is at logic 1, the second output node (Mo) outputs a logic 1 signal.

[Claim 17] 17. The programmable frequency divider of claim 14 further comprising:

- a cell of a second type having a bypass mode and being cascaded to the last cell of the first type, the cell of the second type having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (Rs), a fifth input node (Ci), a first output node (Fo), a second output node (Mo), and a third output node (Co), the first input node (Fi) being coupled to a first output node (Fo) of the last cell of the first type, the second input node (Mi) being coupled to Vcc, the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (Rs) being used for receiving the reset signal to synchronously reset the second cell, the fifth input node (Ci) being used for receiving the last divisor signal, and the second output node (Mo) being coupled to a second input node (Mi) of the last cell of the first type;
- wherein the cell of the second type switches to the divide-by-two or the divide-by-three mode according to the divisor signal received on the third input node (Di) after being synchronously reset, and if the last divisor signal received on

the fifth input node (C_i) is at a bypass-mode active state, the cell of the second type switches to a bypass mode.

[Claim 18] 18. The programmable frequency divider of claim 17 wherein each cell of the second type operates such that:

- (a) regardless of the logic level of the second input node (M_i) or the second output node (M_o), if the first output node (F_o) and the third input node (D_i) are both at logic 0, the positive edge of a clock signal of the first input node (F_i) triggers the first output node (F_o) to output a half frequency signal;
- (b) if the first output node (F_o) is at logic 0, the second input node (M_i) is at logic 1 (or if the second output node (M_o) is at logic 1), and the third input node (D_i) is at logic 1, the positive edge of the clock signal of the first input node (F_i) triggers the first output node (F_o) to output a one-third-frequency signal;
- (c) if the first output node (F_o) is at logic 0, the second output node (M_o) outputs a signal at the same logic level as the second input node (M_i);
- (d) regardless of the logic level of the second input node (M_i), if the first output node (F_o) is at logic 1, the second output node (M_o) outputs a logic 0 signal;
- (e) if the reset signal received on the fourth input node (R_s) is enabled, the first output node (F_o) outputs a logic 0 signal and the second output node (M_o) outputs a logic 1 signal; and
- (f) if the signal received on the fifth input node (C_i) is at an active state, the first output node (F_o) outputs a logic 0 signal and the second output node (M_o) outputs a logic 1 signal.

[Claim 19] 19. The programmable frequency divider of claim 17 further comprising:

at least one cell of a third type having a bypass mode and being cascaded between at least one cell of the first type and the cell of the second type, each cell of the third type having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (Rs), a fifth input node (Ci), a first output node (Fo), a second output node (Mo), and a third output node (Co), the first output node (Fo) being coupled to a first input node (Fi) of a subsequent cell, the second input node (Mi) being coupled to a second output node (Mo) of the subsequent cell of the third type, the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (Rs) being used for receiving the reset signal to synchronously reset the third cell, the fifth input node (Ci) being coupled to a third output node (Co) of the subsequent cell and being used for receiving a bypass-mode enabling signal, a first input node (Fi) of a first cell of the third type being coupled to a first output node (Fo) of the last cell of the first type, a second output node (Mo) of the first cell of the third type being coupled to the second input node (Mi) of the last cell of the first type, a first output node (Fo) of a last cell of the third type being coupled to the first input node (Fi) of the cell of the second type, a second input node (Mi) of the last cell of the third type being coupled to the second output node (Mo) of the cell of the second type;

wherein each cell of the third type switches to a divide-by-two or divide-by-three mode according to the divisor signal received on the third input node (Di), and if the bypass-mode enabling signal received on the fifth input node (Ci) is at an active state, the cell of the third type switches to a bypass mode.

[Claim 20] 20. The programmable frequency divider of claim 19 wherein each cell of the third type operates such that:

- (a) regardless of the logic level of the second input node (Mi) or the second output node (Mo), if the first output node (Fo) and the third input node (Di) are both at logic 0, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the first output node (Fo) is at logic 0, the second input node (Mi) is at logic 1 (or if the second output node (Mo) is at logic 1), and the third input node (Di) is at logic 1, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal;
- (e) if the reset signal received on the fourth input node (Rs) is enabled, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal; and
- (f) if the bypass-mode enabling signal received on the fifth input node (Ci) is at an active state, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal.

[Claim 21] 21. The programmable frequency divider of claim 14 further comprising a control circuit for providing the reset signal.

[Claim 22] 22. A programmable frequency divider for dividing the frequency of a source signal according to a selectable divisor which is obtained based on a plurality of divisor signals and outputting a result signal having a divided frequency, the programmable frequency divider comprising:

at least one cell of a fourth type being switchable between divide-by-two and divide-by-three modes having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (Ri), a first output node (Fo), and a second output node (Mo), the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (Ri) being used for receiving a reload signal to synchronously reload the corresponding divisor signal to the third input node (Di);

wherein if the programmable frequency divider comprising a plurality of cells of the fourth type, the cells of the fourth type being cascaded with each other, the first output node (Fo) being coupled to a first input node (Fi) of a subsequent cell of the fourth type, the second input node (Mi) being coupled to a second output node (Mo) of the subsequent cell of the fourth type, a first input node (Fi) of a first cell of the fourth type being coupled to the source signal, and a second input node (Mi) of a last cell of the fourth type being set to logic 1; the programmable frequency divider synchronously reloads the corresponding divisor signals to the third input node (Di) of each cell of the fourth type according to the reload signal in order to selectively switch each cell of the fourth type to perform a divide-by-two or divide-by-three operation, and the second output node (Mo) or the first output node (Fo) of the last cell of the fourth type outputs the result signal having the divided frequency.

[Claim 23] 23. The programmable frequency divider of claim 22 wherein each cell of the fourth type operates such that:

- (a) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 0 and the third input node (Di) is at logic 0 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the second input node (Mi) is at logic 1, the first output node (Fo) is at logic 0, and the third input node (Di) is at logic 1 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi); and
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal.

[Claim 24] 24. The programmable frequency divider of claim 22 wherein each cell of the fourth type operates such that:

- (a) regardless of the logic level of the second output node (Mo), if the third input node (Di) is at logic 0 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the second output node (Mo) is at logic 1 and the third input node (Di) is at logic 1 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock

- signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi); and
 - (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal.

[Claim 25] 25. The programmable frequency divider of claim 22 wherein the fourth input node (RI) of each cell of the fourth type is coupled to a second output node (Mo) of the last cell of the fourth type in order to apply the result signal having the divided frequency to be the reload signal.

[Claim 26] 26. The programmable frequency divider of claim 22 further comprising:

- a cell of a fifth type having a bypass mode and being cascaded to the last cell of the fourth type, the cell of the fifth type having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (RI), a fifth input node (Ci), a first output node (Fo), a second output node (Mo), and a third output node (Co), the first input node (Fi) being coupled to a first output node (Fo) of the last cell of the fourth type, the second input node (Mi) being coupled to Vcc, the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (RI) being used for receiving the reload signal to synchronously reload the corresponding divisor signal to the third input node (Di), the fifth input node (Ci) being coupled to the last divisor signal, and the second output node (Mo) being coupled to the second input node (Mi) of the last cell of the fourth type;

wherein the reload signal triggers the cell of the fifth type to synchronously reload the corresponding divisor signal to the third input node (Di) and the cell of the fifth type switches to a divide-by-two or divide-by-three mode according to the divisor signal, and if the last divisor signal received in the fifth input node (Ci) is at a bypass-mode active state, the cell of the fifth type switches to a bypass mode.

[Claim 27] 27. The programmable frequency divider of claim 26 wherein each cell of the fifth type operates such that:

- (a) regardless of the logic level of the second input node (Mi) or the second output node (Mo), if the first output node (Fo) is at logic 0 and the third input node (Di) is at logic 0 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the first output node (Fo) is at logic 0, the second input node (Mi) is at logic 1 (or if the second output node (Mo) is at logic 1), and the third input node (Di) is at logic 1 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal; and

(e) if the signal received in the fifth input node (Ci) is at an active state, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal.

[Claim 28] 28. The programmable frequency divider of claim 26, wherein the fourth input node (RI) of the cell of the fifth type is coupled to the second output node (Mo) of the last cell of the fourth type in order to apply the result signal having the divided frequency to be the reload signal.

[Claim 29] 29. The programmable frequency divider of claim 26, further comprising:

at least one cell of a sixth type having a bypass mode and being cascaded between at least one cell of the fourth type and the cell of the fifth type, each cell of the sixth type having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (RI), a fifth input node (Ci), a first output node (Fo), a second output node (Mo), and a third output node (Co), the first output node (Fo) being coupled to a first input node (Fi) of a subsequent cell, the second input node (Mi) being coupled to a second output node (Mo) of the subsequent cell, the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (RI) being used for receiving the reload signal to synchronously reload the the corresponding divisor signal to the third input node (Di), the fifth input node (Ci) being coupled to a third output node (Co) of the subsequent cell and being used for receiving a bypass-mode enabling signal, a first input node (Fi) of a first cell of the sixth type being coupled to the first output node (Fo) of the last cell of the fourth type, a second output node (Mo) of the first cell of the sixth type being coupled to the second input node (Mi) of the last cell of the fourth type, a first output node (Fo) of a last

cell of the sixth type being coupled to the first input node (Fi) of the cell of the fifth type, and a second input node (Mi) of the last cell of the sixth type being coupled to the second output node (Mo) of the cell of the fifth type;

wherein the reload signal triggers the at least one cell of the sixth type to synchronously reload the corresponding divisor signal to the third input node (Di) and each cell of the sixth type switches to a divide-by-two or divide-by-three mode according to the respective divisor signal, and if the bypass-mode enabling signal received in the fifth input node (Ci) is at an active state, the cell of the sixth type switches to a bypass mode.

[Claim 30] 30. The programmable frequency divider of claim 29, wherein each cell of the sixth type operates such that:

- (a) regardless of the logic level of the second input node (Mi) or the second output node (Mo), if the first output node (Fo) is at logic 0 and the third input node (Di) is at logic 0 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the first output node (Fo) is at logic 0, the second input node (Mi) is at logic 1 (or if the second output node (Mo) is at logic 1), and the third input node (Di) is at logic 1 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal having the same logic level as the second input node (Mi);

- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal; and
- (e) if the bypass-mode enabling signal received on the fifth input node (Ci) is at an active state, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal.

[Claim 31] 31. The programmable frequency divider of claim 29, wherein the fourth input node (Ri) of each cell of the sixth type is coupled to the second output node (Mo) of the last cell of the fourth type in order to apply the result signal having the divided frequency to be the reload signal.

[Claim 32] 32. A programmable frequency divider for dividing the frequency of a source signal according to a selectable divisor which is obtained based on a plurality of divisor signals and outputting a result signal having a divided frequency, the programmable frequency divider comprising:

- at least one cell of a seventh type being switchable between divide-by-two and divide-by-three modes having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (Rs), a fifth input node (Ri), a first output node (Fo), and a second output node (Mo), the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (Rs) being used for receiving a reset signal to synchronously reset the cell of the seventh type, the fifth input node (Ri) being used for receiving a reload signal to synchronously reload the corresponding divisor signal to the third input node (Di);
- wherein if the programmable frequency divider comprising a plurality of cells of the seventh type, the cells of the seventh type being cascaded with each other and each cell of the seventh type, the first output node (Fo) being coupled to a

first input node (Fi) of a subsequent cell of the seventh type, the second input node (Mi) being coupled to a second output node (Mo) of the subsequent cell of the seventh type, a first input node (Fi) of a first cell of the seventh type being coupled to the source signal, and a second input node (Mi) of a last cell of the seventh type being set to logic 1; the programmable frequency divider reloads the corresponding divisor signal to the third input node (Di) of each cell of the seventh type according to the reload signal and resets each cell of the seventh type according to the reset signal in order to selectively switch each cell of the seventh type to perform a divide-by-two or divide-by-three operation according to the respective divisor signal loaded before reset, and the second output node (Mo) or the first output node (Fo) of the last cell of the seventh type outputs the result signal having the divided frequency.

[Claim 33] 33. The programmable frequency divider of claim 32, wherein each cell of the seventh type operates such that:

- (a) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 0 and the third input node (Di) is at logic 0 when the fifth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the second input node (Mi) is at logic 1, the first output node (Fo) is at logic 0, and the third input node (Di) is at logic 1 when the fifth input node (Ri) is triggered by the reload signal, the positive edge of the clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;

- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal; and
- (e) if the reset signal received on the fourth input node (Rs) is at logic 1, the first output node (Fo) outputs a logic 0 signal; and, additionally, if the second input node (Mi) is also at logic 1, the second output node (Mo) outputs a logic 1 signal.

[Claim 34] 34. The programmable frequency divider of claim 32, wherein each cell of the seventh type operates such that:

- (a) regardless of the logic level of the second output node (Mo), if the third input node (Di) is at logic 0 when the fifth input node (RI) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the second output node (Mo) is at logic 1 and the third input node (Di) is at logic 1 when the fifth input node (RI) is triggered by the reload signal, the positive edge of the clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic signal as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal; and
- (e) if the reset signal received on the fourth input node (Rs) is enabled, the first output node (Fo) outputs a logic 0 signal;

and, additionally, if the second input node (M_i) is also at logic 1, the second output node (M_o) outputs a logic 1 signal.

[Claim 35] 35. The programmable frequency divider of claim 32, wherein the fifth input node (R_l) of each cell of the seventh type is coupled to the second output node (M_o) of the last cell of the seventh type in order to apply the result signal to be the reload signal.

[Claim 36] 36. The programmable frequency divider of claim 32, further comprising a control circuit for providing the reset signal.

[Claim 37] 37. The programmable frequency divider of claim 32, further comprising:

- a cell of an eighth type having a bypass mode and being cascaded to the last cell of the seventh type, the cell of the eighth type having a first input node (F_i), a second input node (M_i), a third input node (D_i), a fourth input node (R_s), a fifth input node (R_l), a sixth input node (C_i), a first output node (F_o), a second output node (M_o), and a third output node (C_o), the first input node (F_i) being coupled to a first output node (F_o) of the last cell of the seventh type, the second input node (M_i) being coupled to V_{cc} , the third input node (D_i) being used for receiving a corresponding divisor signal, the fourth input node (R_s) being used for receiving the reset signal to reset the cell of the eighth type, the fifth input node (R_l) being used for receiving the reload signal to synchronously reload the corresponding divisor signal to the third input node (D_i), the sixth input node (C_i) being coupled to the last divisor signal, and the second output node (M_o) being coupled to the second input node (M_i) of the last cell of the seventh type;

wherein the reload signal triggers the cell of the eighth type to synchronously reload the corresponding divisor signal to the third input node (Di) and the cell of the eighth type switches to a divide-by-two or a divide-by-three mode after being synchronously reset according to the divisor signal, and if the last divisor signal received on the sixth input node (Ci) is at a bypass-mode active state, the cell of the eighth type switches to a bypass mode.

[Claim 38] 38. The programmable frequency divider of claim 37, wherein each cell of the eighth type operates such that:

- (a) regardless of the logic level of the second input node (Mi) or the second output node (Mo), if the first output node (Fo) is at logic 0, and the third input node (Di) is at logic 0 when the fifth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the first output node (Fo) is at logic 0, the second input node (Mi) is at logic 1 (or if the second output node (Mo) is at logic 1), and the third input node (Di) is at logic 1 when the fifth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal;

- (e) if the reset signal received on the fourth input node (Rs) is enabled, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal; and
- (f) if the signal received on the sixth input node (Ci) is at an active state, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal.

[Claim 39] 39. The programmable frequency divider of claim 37, wherein the fifth input node (RI) is coupled to the second output node (Mo) of the last cell of the seventh type in order to apply the result signal to be the reload signal.

[Claim 40] 40. The programmable frequency divider of claim 37, further comprising:

at least one cell of a ninth type having a bypass mode and being cascaded between at least one cell of the seventh type and the cell of the eighth type, each cell of the ninth type having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (Rs), a fifth input node (RI), a sixth input node (Ci), a first output node (Fo), a second output node (Mo), and a third output node (Co), the first output node (Fo) being coupled to a first input node (Fi) of a subsequent cell of the ninth type, the second input node (Mi) being coupled to a second output node (Mo) of the subsequent cell, the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (Rs) being used for receiving the reset signal to synchronously reset the cell of the ninth type, the fifth input node (RI) being used for receiving the reload signal to synchronously reload the corresponding divisor signal to the

third input node (Di), the sixth input node (Ci) being coupled to a third output node (Co) of the subsequent cell and being used for receiving a bypass-mode enabling signal, a first input node (Fi) of a first cell of the ninth type being coupled to the first output node (Fo) of the last cell of the seventh type, a second output node (Mo) of the first cell of the ninth type being coupled to the second input node (Mi) of the last cell of the seventh type, a first output node (Fo) of a last cell of the ninth type being coupled to the first input node (Fi) of the cell of the eighth type, and a second input node (Mi) of the last cell of the ninth type being coupled to the second output node (Mo) of the cell of the eighth type;

wherein the reload signal triggers the at least one cell of the ninth type to synchronously reload the corresponding divisor signal to the third input node (Di) and each cell of the ninth type switches to a divide-by-two or divide-by-three mode after being synchronously reset according to the respective divisor signal, and if the bypass-mode enabling signal received on the sixth input node (Ci) is at an active state, the cell of the ninth type switches to a bypass mode.

[Claim 41] 41. The programmable frequency divider of claim 40, wherein each cell of the ninth type operates such that:

- (a) regardless of the logic level of the second input node (Mi) or the second output node (Mo), if the first output node (Fo) is at logic 0 and the third input node (Di) is at logic 0 when the fifth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the first output node (Fo) is at logic 0, the second input node (Mi) is at logic 1 (or if the second output node (Mo) is at

logic 1), and the third input node (Di) is at logic 1 when the fifth input node (Ri) triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;

- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal;
- (e) if the reset signal received on the fourth input node (Rs) is enabled, the first output node (Fo) outputs a logic 0 signal; and, additionally, if the second input node (Mi) is also at logic 1, the second output node (Mo) outputs a logic 1 signal; and
- (f) if the bypass-mode enabling signal received on the sixth input node (Ci) is at an active state, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal.

[Claim 42] 42. The programmable frequency divider of claim 40, wherein the fifth input node (Ri) of each cell of the ninth type is coupled to the second output node (Mo) of the last cell of the seventh type in order to apply the result signal to be the reload signal.

[Claim 43] 43. A programmable frequency divider for dividing frequency of a source signal according to a selectable divisor which is obtained based on a plurality of divisor signals and outputting a result signal having a divided frequency, the programmable frequency divider comprising:

at least one cell of a tenth type being switchable between divide-by-two and divide-by-three modes having a first input node (Fi), a second input node (Mi), a third input node (Di), a first

output node (Fo), and a second output node (Mo), the third input node (Di) being used for receiving a corresponding divisor signal, and the first input node (Fi) of a first cell of the tenth type being coupled to the source signal; and

a cell of an eleventh type having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (RI), a fifth input node (Ci), a first output node (Fo), a second output node (Mo), and a third output node (Co), the first input node (Fi) being coupled to a first output node (Fo) of a last cell of the tenth type, the second input node (Mi) being set to logic 1, the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (RI) being used for receiving a reload signal to synchronously reload the corresponding divisor signal to the third input node (Di), the fifth input node (Ci) being coupled to a last divisor signal, and the second output node (Mo) being coupled to a second input node (Mi) of the last cell of the tenth type;

wherein if the programmable frequency divider comprising a plurality of cells of the tenth type, the cells of the tenth type being cascaded with each other and each cell of the tenth type, the first output node (Fo) being coupled to a first input node (Fi) of a subsequent cell of the tenth type, the second input node (Mi) being coupled to a second output node (Mo) of the subsequent cell of the tenth type; the programmable frequency divider selectively switches each cell to a divide-by-two or a divide-by-three mode according to the respective divisor signal, the reload signal triggers the third input node (Di) of the cell of the eleventh type to reload the corresponding divisor signal, if the last divisor signal received in the fifth input node (Ci) of the cell of the eleven type is at a bypass-mode active state, the cell of the eleventh type switches to a bypass mode, and the second output node (Mo)

or the first output node (Fo) of the last cell of the tenth type outputs the result signal having the divided frequency.

[Claim 44] 44. The programmable frequency divider of claim 43, wherein each cell of the tenth type operates such that:

- (a) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 0 and the third input node (Di) is at logic 0, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the second input node (Mi) is at logic 1, the first output node (Fo) is at logic 0, and the third input node (Di) is at logic 1, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi); and
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal.

[Claim 45] 45. The programmable frequency divider of claim 43, wherein each cell of the tenth type operates such that:

- (a) regardless of the logic level of the second output node (Mo), if the third input node (Di) is at logic 0, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the second output node (Mo) and the third input node (Di) are both at logic 1, the positive edge of the clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;

- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi); and
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal.

[Claim 46] 46. The programmable frequency divider of claim 43, wherein the cell of the eleventh type operates such that:

- (a) regardless of the logic level of the second input node (Mi) or the second output node (Mo), if the first output node (Fo) is at logic 0 and the third input node (Di) is at logic 0 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the first output node (Fo) is at logic 0, the second input node (Mi) is at logic 1 (or if the second output node (Mo) is at logic 1), and the third input node (Di) is at logic 1 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal; and
- (e) if the signal received on the fifth input node (Ci) is at an active state, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal.

[Claim 47] 47. The programmable frequency divider of claim 43, wherein the fourth input node (RI) of the cell of the eleventh type is coupled to the second output node (Mo) of the last cell of the tenth type in order to apply the result signal to be the reload signal.

[Claim 48] 48. The programmable frequency divider of claim 43, further comprising:

at least one cell of a twelfth type being cascaded between at least one cell of the tenth type and the cell of the eleventh type, and each cell of the twelfth type having a first input node (Fi), a second input node (Mi), a third input node (Di), a fourth input node (RI), a fifth input node (Ci), a first output node (Fo), a second output node (Mo), and a third output node (Co), the first output node (Fo) being coupled to a first input node (Fi) of a subsequent cell of the twelfth type, the second input node (Mi) being coupled to a second output node (Mo) of the subsequent cell, the third input node (Di) being used for receiving a corresponding divisor signal, the fourth input node (RI) being used for receiving the reload signal to synchronously reload the corresponding divisor signal to the third input node (Di), the fifth input node (Ci) being coupled to a third output node (Co) of the subsequent cell and being used for receiving a bypass-mode enabling signal, a first input node (Fi) of a first cell of the twelfth type being coupled to the first output node (Fo) of the last cell of the tenth type, a second output node (Mo) of the first cell of the twelfth type being coupled to the second input node (Mi) of the last cell of the tenth type, a first output node (Fo) of a last cell of the twelfth type being coupled to the first input node (Fi) of the cell of the eleventh type, and a second input node (Mi) of the

last cell of the twelfth type being coupled to the second output node (Mo) of the cell of the eleventh type;

wherein the reload signal triggers each cell of the twelfth type to synchronously reload the corresponding divisor signal to the third input node (Di), each cell of the twelfth type switches to a divide-by-two or divide-by-three mode according to the loaded divisor signal, and if the bypass-mode enabling signal received on the fifth input node (Ci) is at an active state, the cell of the twelfth type switches to a bypass mode.

[Claim 49] 49. The programmable frequency divider of claim 48, wherein each cell of the twelfth type operates such that:

- (a) regardless of the logic level of the second input node (Mi) or the second output node (Mo), if the first output node (Fo) is at logic 0 and the third input node (Di) is at logic 0 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of a clock signal of the first input node (Fi) triggers the first output node (Fo) to output a half frequency signal;
- (b) if the first output node (Fo) is at logic 0, the second input node (Mi) is at logic 1 (or if the second output node (Mo) is at logic 1), and the third input node (Di) is at logic 1 when the fourth input node (Ri) is triggered by the reload signal, the positive edge of the clock signal of the first input node (Fi) triggers the first output node (Fo) to output a one-third-frequency signal;
- (c) if the first output node (Fo) is at logic 0, the second output node (Mo) outputs a signal at the same logic level as the second input node (Mi);
- (d) regardless of the logic level of the second input node (Mi), if the first output node (Fo) is at logic 1, the second output node (Mo) outputs a logic 0 signal; and

- (e) if the bypass-mode enabling signal received on the fifth input node (Ci) is at an active state, the first output node (Fo) outputs a logic 0 signal and the second output node (Mo) outputs a logic 1 signal.

[Claim 50] 50. The programmable frequency divider of claim 48, wherein the fourth input node (RI) of each cell of the twelfth type is coupled to the second output node (Mo) of the last cell of the tenth type in order to apply the result signal to be the reload signal.